

METHOD AND CIRCUIT FOR MULTIPLYING SIGNALS WITH A TRANSISTOR HAVING MORE THAN ONE INDEPENDENT GATE STRUCTURE

RELATED APPLICATIONS

5 This application is related to the application entitled "Transistor With Independent Gate Structure", by Mathew et al., having application number 10/443,375, filed on May 22, 2003, and assigned to the assignee hereof.

 This application is related to the application entitled "Memory With Charge Storage Locations", by Mathew et al., having application Number 10/443,908, filed on May 22, 2003,
10 and assigned to the assignee hereof.

FIELD OF THE INVENTION

 This invention relates generally to mixers and more specifically to a method for mixing signals with a transistor having more than one independent gate structure.

BACKGROUND OF THE INVENTION

15 A mixer circuit is a type of multiplier circuit that provides frequency translation for two or more signals. For example, in a radio receiver, a mixer circuit is used to translate an RF (radio frequency) signal to an IF (intermediate frequency) signal. In an integrated circuit mixer, the signals to be mixed are applied to the gates of input transistors. The output is a multiplication of the two input signals. Designers of high frequency mixer circuits have been faced with the
20 problem of providing a relatively small and easy to implement mixer circuit that provides highly linear operation at low power supply voltages (e. g. 1.0 - 1.5 volts).

 Therefore, it is desirable to provide an integrated circuit device for mixing two signals that is small and easy to implement, yet provides highly linear operation at low voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings. The use of the same reference symbols in different drawings indicates identical items unless
5 otherwise noted.

FIG. 1 is a partial side cross sectional view of one embodiment of a semiconductor wafer during a stage in the manufacture of a transistor according to the present invention.

FIG. 2 is a partial side cross sectional view of one embodiment of a semiconductor wafer during another stage in the manufacture of a transistor according to the present invention.

10 FIG. 3 is a partial isometric view of one embodiment of a semiconductor wafer during another stage in the manufacture of a transistor according to the present invention.

FIG. 4 is a partial side cross sectional view of one embodiment of a semiconductor wafer during another stage in the manufacture of a transistor according to the present invention.

15 FIG. 5 is a partial side cross sectional view of one embodiment of a semiconductor wafer during another stage in the manufacture of a transistor according to the present invention.

FIG. 6 is a partial side cross sectional view of one embodiment of a semiconductor wafer during another stage in the manufacture of a transistor according to the present invention.

FIG. 7 is a partial side cross sectional view of one embodiment of a semiconductor wafer during another stage in the manufacture of a transistor according to the present invention.

20 FIG. 8 is a partial side cross sectional view of one embodiment of a semiconductor wafer during another stage in the manufacture of a transistor according to the present invention.

FIG. 9 is a partial isometric view of one embodiment of a semiconductor wafer during another stage in the manufacture of a transistor according to the present invention.

25 FIG. 10 is a partial side cross sectional view of one embodiment of a semiconductor wafer during another stage in the manufacture of a transistor according to the present invention.

FIG. 11 is a partial side cross sectional view of another embodiment of a semiconductor wafer during a stage in the manufacture of a transistor according to the present invention.

FIG. 12 is a partial side cross sectional view of another embodiment of a semiconductor wafer during another stage in the manufacture of a transistor according to the present invention.

5 FIG. 13 is a partial side cross sectional view of another embodiment of a semiconductor wafer during another stage in the manufacture of a transistor according to the present invention.

FIG. 14 is a partial side cross sectional view of another embodiment of a semiconductor wafer during another stage in the manufacture of a transistor according to the present invention.

10 FIG. 15 is a partial side cross sectional view of another embodiment of a semiconductor wafer during another stage in the manufacture of a transistor according to the present invention.

FIG. 16 is a partial isometric view of another embodiment of a semiconductor wafer during another stage in the manufacture of a transistor according to the present invention.

FIG. 17 is a partial cut away top view of another embodiment of a transistor according to the present invention.

15 FIG. 18 is a schematic of one embodiment of a memory array according to the present invention.

FIG. 19 sets forth a table of one embodiment of a set of voltages applied to bitlines and word lines of a memory array for programming, erasing, and reading a charge storage location of the memory array according to the present invention.

20 FIG. 20 sets forth a table of one embodiment of a set of voltages applied to bitlines and word lines of a memory array for programming, erasing, and reading another charge storage location of the memory array according to the present invention.

FIG. 21 sets forth a table of another embodiment of a set of voltages applied to bitlines and word lines of another memory array for programming, erasing, and reading a charge storage
25 location of the memory array according to the present invention.

FIG. 22 sets forth a table of another embodiment of a set of voltages applied to bitlines and word lines of another memory array for programming, erasing, and reading another charge storage location of the memory array according to the present invention.

FIG. 23 illustrates a schematic diagram of a mixer circuit in accordance with the present invention.

FIG. 24 illustrates a top down layout view of a transistor used in the mixer circuit of FIG. 23.

DETAILED DESCRIPTION

Generally, the present invention provides a multiplier circuit. The multiplier circuit includes a semiconductor “fin” formed on a substrate. The fin has first and second sidewalls. A layer of gate material is formed over the substrate and the fin, the gate material including a first portion adjacent to the first sidewall of the fin and a second portion adjacent to the second sidewall of the fin. The layer of gate material is removed from over the semiconductor fin to leave a first gate along the first sidewall and a second gate along the second sidewall, where the first and second gates have a predetermined height and are electrically isolated from each other. The first and second gates function as input terminals for the multiplier circuit and a first input signal is applied to the first gate and a second input signal to be multiplied with the first input signal is applied to the second gate. In another embodiment, the multiplier circuit functions as a mixer circuit.

A mixer circuit in accordance with the present invention provides the advantages of having fully symmetrical independent input gates. Also, the transistor does not suffer from unpredictable body effects such as floating body and source-drain coupling of back bias. In addition, the gate lengths of the transistors may be changed without a fabrication process change, providing a highly linear mixer that may be integrated in a multi-functional system on a chip (SoC) integrated circuit. Further, because a transistor stack is not used as in some prior art mixers, the mixer circuit can operate at low power supply voltages.

The following sets forth a detailed description of a mode for carrying out the invention. The description is intended to be illustrative of the invention and should not be taken to be limiting.

FIG. 1 shows a partial side cross sectional view of one embodiment of a semiconductor wafer during a stage in the manufacture of a transistor with independent gate structures according to the present invention. Wafer 101 includes a substrate with an insulating layer 103. A structure 104 has been formed over insulating layer 103. Structure 104 includes a semiconductor structure portion 105 formed over insulating layer 103, a dielectric portion 111 (e.g. silicon dioxide) formed over semiconductor structure portion 105 and layer 103, and a nitride portion 109 located over portion 111 and portion 105. In one embodiment, structure 104 is formed by depositing a layer of semiconductor material over layer 103, forming a dielectric layer over the semiconductor layer (e.g. by thermal oxidation of the semiconductor layer or by atomic layer deposition of a high K dielectric), and then depositing a layer of nitride over the dielectric. The semiconductor layer, the dielectric layer, and the nitride layer are then patterned to form structure 104. Afterwards, a dielectric layer 106 is formed on the sidewalls of semiconductor structure portion 105. As will be shown later, a channel region and current terminal regions of a transistor are formed in semiconductor structure portion 105 of structure 104. In one embodiment, semiconductor structure portion 105 is made of epitaxial silicon bonded on insulating layer 103. In other embodiments, portion 105 may be made of polysilicon or other semiconductor material. In one embodiment, structure 104 is a fin structure of a FinFET. In other embodiments, portion 109 may be made of other materials (e.g. other dielectrics) that can be utilized as a hard etch mask.

Referring to FIG. 2, a conformal polysilicon layer 203 is deposited over wafer 101 including over structure 104. As will be shown later, polysilicon layer 203 is utilized to form independent gate structures of a FinFET transistor. In other embodiments, layer 203 may be made of other gate materials such as e.g. tungsten, titanium, tantalum silicon nitride, silicides such as cobalt or nickel silicides, germanium, silicon germanium, other metals, or combinations thereof. In the embodiment shown, a conformal nitride layer 205 is then deposited over layer 203. In one embodiment, layer 205 is used both as an antireflective coating and as a hard mask for etching layer 203. Layer 205 may not be included in some embodiments. In some

embodiments, layer 203 may be doped prior to the deposition of layer 205. In these embodiments, layer 205 may be doped with single or multiple implants at various energies, angles, and/or species. For example, in one embodiment, the left side of layer 203, relative to the view shown in FIG. 2, may be doped with a first dopant at a first angle to provide that portion with a first conductivity type, and the right side of the layer 203, relative to the view shown in FIG. 2 may be doped at a second angle relative to the view shown in FIG. 2 to provide that portion with a second conductivity type.

FIG. 3 is a partial isometric view of wafer 101 after layers 205 and 203 have been patterned to form gate structure 301. In some embodiments, layers 205 and 203 are patterned by the utilization of conventional photolithographic techniques. During the patterning, the portion of nitride portion 109 located over structure 104 but not located under gate structure 301 is removed. In other embodiments, this portion of nitride portion 109 may be removed at a later stage during manufacture.

Structure 104 includes current terminal regions 303 and 305 located in each end of portion 105 of structure 104. In one embodiment where the resultant transistor structure is a field effect transistor (FET), regions 303 and 305 serve as the source and drain regions, respectively. Regions 303 and 305 may be doped at this time by e.g. ion implantation or plasma doping.

FIG. 4 shows a partial cross sectional view of wafer 101 after a deposition of a planar layer 403 over wafer 101. In some embodiments, layer 403 may be made of e.g., photo resist, spin on glass, or organic antireflective coating material. Layer 403 may be formed by spin on techniques or by chemical vapor deposition techniques followed by chemical mechanical polish or reflow.

FIG. 5 shows wafer 101 after layer 403 has been etched back to a level below the top of portion 505 of nitride layer 203 located over structure 104 to expose portion 505. In one embodiment, layer 403 may be etched back, e.g., by a conventional dry or wet etch techniques. In the embodiment shown, after the etch back, layer 403 is at least thick enough to cover portion 503 of layer 205 such that portion 505 of layer 205 may be removed by etching without removing portion 503.

In other embodiments, the resultant structure of layer 403 as shown in FIG. 5 may be formed by the planar deposition of the material of layer 403 to the level shown in FIG. 5, or other desired level.

5 FIG. 6 shows the same view as FIG. 5 after portion 505 of nitride layer 205 located over structure 104 has been removed by etching. Layer 403, as shown in FIG. 6, protects portion 503 of layer 205 from being removed during the etching of portion 505.

Referring to FIG. 7, after portion 505 of layer 205 has been removed, the portion of layer 203 previously located under removed portion 505 of layer 205 is removed by a non abrasive etching (e.g. wet or dry) to form independent gate structures 701 and 703. Layer 403 (along with
10 the remaining portions of layer 205) protects portions 707 and 709 of layer 203 from being removed during the etching of layer 203. Gate structures 701 and 703 each have a vertical portion located along a sidewall of structure 104.

Utilizing a planar layer for the formation of independent gate structures may allow a portion of the gate material to be removed to form separate gate structures for a transistor
15 without extra masking steps. In some embodiments, the planar layer allows for the portion of the gate structure located over structure 104 to be removed without removing the portions of the gate structure used to form the independent gate structures. In some embodiments, because portions of the conformal layers including the gate material located over structure 104 are exposed from the planar layer, those portions can be removed e.g. by etching to isolate the gate structures
20 without use of an extra mask step. Accordingly, alignment problems in forming separate gates may be avoided.

FIG. 8 shows the same view as FIG. 7 after the removal of the remaining portions of layers 403 and 205. In some embodiments, these layers may be removed by wet or dry etches. In other embodiments, the remaining portions of layers 403 and 205 are not removed.

25 FIG. 9 shows an isometric view of the transistor shown in FIG. 8. In later processing stages, spacers and silicide layers of the transistor are formed by conventional semiconductor techniques. Regions 903 and 905 serve as current terminal contacts (e.g. as source/drain contacts

for FETs). Also, regions 907 and 909 serve as gate contacts for gate structures 701 and 703, respectively.

FIG. 10 shows the same view as FIG. 8 after the formation of gate vias 1003 and 1005 over regions 907 and 909, respectively. A low K dielectric material 1009 is shown deposited over the resultant transistor structure. Other conventional processing stages not shown or described herein may be performed on wafer 101 to form other conventional structures (such as e.g. interconnects and passivation layers) of a semiconductor device. Afterwards, the wafer is singulated to separate the integrated circuits of the wafer.

Transistors with independent gate structures according to the present invention may be made by other processes. For example, the formation of the planar layer 403 and the removal of the portion of gate material (e.g. in layer 203) located over structure 104 may be performed after the formation of spacers and/or silicides as described above with respect to FIG. 10. Also, transistors with independent gate structures may be made without utilizing conformal nitride layer 205. With these embodiments, the planar layer 403 would be formed such that the top portion of the layer of gate material (e.g. 203) located over structure 104 would be exposed for etching.

In some embodiments, independent gate structures may be coupled together either by hardwiring (e.g. conductive material extending between the gate structures) or by other transistors which would allow for the gate structures to be selectively coupled together.

FIGs. 11-17 set forth views of a semiconductor wafer during various stages in the manufacture of another embodiment of a transistor with independent gate structures according to the present invention. The transistor formed also includes charge storage locations located between the gates and the channel region of the transistor. As will be described later, such a transistor may be utilized as a non volatile memory device for storing data in the charge storage locations.

Wafer 1101 includes a substrate having an insulating layer 1103. A structure 1104 has been formed over insulating layer 1103. In one embodiment, structure 1104 is a "fin" structure for a FinFET transistor having charge storage locations. Structure 1104 includes a

semiconductor structure portion 1105 formed over the insulating layer 1103, a dielectric portion 1111 (e.g. silicon dioxide) formed over semiconductor structure portion 1105 and layer 1103, and a nitride portion 1109 located over portion 1111 and portion 1105. In one embodiment, structure 1104 is formed by depositing a layer of semiconductor material over layer 1103, forming a dielectric layer over the semiconductor material layer (e.g. by thermal oxidation of the semiconductor layer or by atomic layer deposition of a high K dielectric), and then depositing a layer of nitride over the dielectric. The semiconductor layer, the dielectric layer, and the nitride layer are then patterned to form a structure wherein the sidewalls of the semiconductor layer, the dielectric portion 1111, and nitride portion 1109 are flush with each other. In the embodiment shown, the remaining portion of the semiconductor layer is then trimmed (e.g. with a dry etch having an isotropic component) to recess the sidewalls of remaining semiconductor layer to form portion 1105 as shown in FIG. 11. In other embodiments, structure portion 1105 is not trimmed. In some embodiments, structure portion 1105 may be doped prior to the patterning of the layer of semiconductor material by conventional semiconductor processing techniques to provide the channel region of portion 105 with a specific conductivity type.

Afterwards, a dielectric layer 1107 is formed on the sidewalls of semiconductor structure portion 1105. As will be shown later, the channel region and current terminal regions are formed in portion 1105. In one embodiment, semiconductor structure portion 1105 is made of epitaxial silicon bonded on insulating layer 1103. In other embodiments, portion 1105 may be made of polysilicon or other semiconductor material. In one embodiment, structure 1104 is a fin structure of a FinFET.

Referring to FIG. 12, a layer 1203 of charge storage material is then deposited over wafer 1101 including structure 1104. In one embodiment, layer 1203 includes a layer of conductive material such as polysilicon (e.g. as with a floating gate transistor). In other embodiments, layer 1203 may include other types of charge storage material including material having a plurality of charge trapping elements (e.g. silicon nitride as with a thin film transistor). Still in other embodiments, layer 1203 may include discrete charge storage material (e.g. silicon nanocrystals embedded in a layer of dielectric). In some embodiments, the nanocrystals are 2-10 nm in diameter and have a density of $3 \cdot 10^{11}/\text{cm}^2$. In other embodiments, layer 1203 may be made of multiple layers such as e.g. a layer of silicon nanocrystals and a layer of silicon nitride

deposited over the layer of silicon nanocrystals or a layer of silicon nanocrystals embedded between two layers of dielectric material.

FIG. 13 shows a partial cross sectional view of wafer 1101 after layer 1203 has been etched to remove the portion of layer 1203 located over nitride portion 1109 and located on insulating layer 1103. Portions of layer 1203 remaining will later be etched to form isolated charge storage structures 1307 and 1305 located on the opposite sidewalls of structure 1104. In one embodiment, layer 1203 is etched with anisotropic dry etch to form storage structures 1307 and 1305. In some embodiments, where the charge storage material is made of a high resistivity material such that there would be little to no leakage current, layer 1203 is not etched. In such embodiments, the charge storage structures having charge storage locations would be part of a contiguous layer 1203.

FIG. 14 shows a partial cross sectional view of wafer 1101 after a conformal layer 1403 of control dielectric has been deposited over wafer 1101 and after a conformal layer 1407 of gate material has been deposited over layer 1403.

After the deposition of gate material layer 1407, the wafer is further processed to form two gate structures as per a similar process described above with respect to FIGs 2-8. For example, a nitride layer (not shown), similar to nitride layer 205 in FIG. 2, is deposited over layer 1407. The nitride layer and layer 1407 is then patterned to form a gate structure similar to gate structure 301 shown in FIG. 3. In some embodiments, a portion of charge storage layer 1203 located on the side of dielectric layer 1107 and not underneath the gate structure is etched after the layer 1407 has been etched. After the formation of a gate structure, a planar layer (similar to layer 403 in FIG. 5) is formed wherein the portion of the nitride layer located above structure 1104 is exposed (See FIG. 5 and the text discussing thereof). After the removal of the exposed portion of the nitride layer, the gate material located above structure 1104 is then etched to form gate structures 1505 and 1503 (See FIG. 15) in a manner similar to that set forth in FIGs. 6-8 and the discussion thereof.

FIG. 15 shows a partial side view of wafer 1101 after the formation of gate structures 1505 and 1503. FIG. 16 is a partial isometric view of the transistor structure shown in FIG. 15. Regions 1607 and 1605 serve as current terminal regions with 1611 and 1613 serving as current

terminal contacts (e.g. as source/drain contacts for FETs) for those regions. Also, regions 1620 and 1617 serve as gate contacts for gate structures, 1505 and 1503 respectively.

5 In some embodiments, gate structures 1503 and 1505 are doped. The material of these gate structures is doped, in one embodiment, prior to the deposition of the nitride layer (e.g. 205) over the layer of gate material. Also, in some embodiments, the current terminal regions 1607 and 1605 are doped after the formation of gate structures 1505 and 1503 to provide a conductivity type that is different from the conductivity type of the channel region of semiconductor structure portion 1105.

10 In later processing stages, silicide layers, spacers, gate vias, and current terminal vias and are formed over transistor structure 1621 by conventional semiconductor techniques. A low K dielectric material (e.g. 1009) may also be deposited over the resultant transistor structure 1621. Other conventional processing stages not shown or described herein may be performed on wafer 1101 to form other conventional structures (such as e.g. interconnects and passivation layers) of an integrated circuit.

15 The resultant transistor structure 1621 shown in FIG. 16 can be utilized as a non volatile memory cell having four isolated charge storage locations (two each in charge storage structure 1305 and 1307, respectively) that can each store one of bit of data.

FIG. 17 is a partial cutaway top view of transistor structure 1621 shown in FIG. 16. Charge storage structure 1305 includes two charge storage locations 1709 and 1711, and charge
20 structure 1307 includes two charge storage locations 1713 and 1715. These four charge storage locations may be programmed, read, and or erased by applying voltages to current terminal regions 1605 and 1607 and gate structures 1503 and 1505.

In one embodiment, the transistor structure 1621 functions as two functional MOSFET transistors that share source/drain regions and each have two charge storage locations. Gate
25 structure 1503 serves as the gate for one of the functional transistors, and gate structure 1505 serves as the gate of the other functional transistors. Charge storage locations 1709 and 1711 serve as charge storage locations for the functional transistor having gate structure 1503 as its

gate. Charge storage locations 1713 and 1715 serve as charge storage locations for the functional transistor having gate structure 1505 as its gate.

5 In the embodiment shown, semiconductor structure portion 1105 includes a channel region 1725 (approximately differentiated by the dashed lines) located between current terminal regions 1605 and 1607. Channel region 1725 is doped to provide a first conductivity type and current terminal regions 1605 and 1607 are doped to provide a second conductivity type.

10 During the operation of transistor structure 1621, when a voltage is applied to gate structure 1503 that exceeds a voltage threshold of the functional transistor associated with gate structure 1503, an inversion region forms along the sidewall of the channel region 1725 adjacent to gate structure 1503. When a voltage is applied to gate structure 1505 that exceeds a voltage threshold of the functional transistor associated with that gate structure, an inversion layer forms along the sidewall of channel region 1725 adjacent to gate structure 1505. In some embodiments where portion 1105 is relatively thin between gate structures 1503 and 1505, the regions where the inversion layers occur may overlap.

15 Charge may be injected into each of the charge storage locations (e.g. by hot carrier injection) to increase the threshold voltage of the functional transistor associated with that charge storage location. For example, to store a charge in charge storage location 1709, a positive voltage (V_{pp}) is applied to gate structure 1503, $\frac{1}{2} V_{pp}$ is applied to current terminal region 1605, and a ground potential is applied to current terminal region 1607 and gate structure 1505.

20 Each of the charge storage locations may be read independently of each other. Application of a positive voltage (V_{dd}) to the gate structure adjacent to a charge storage location and a positive voltage (V_{dd}) to the current terminal on the opposite side of the charge storage location will effectively read the charge stored in the charge storage location without being affected by the charge stored in the other charge storage locations. For example, to read charge
25 storage location 1709, a positive charge is applied to gate structure 1503 and to current terminal region 1607, with a ground potential (V_{SS}) being applied to gate structure 1505 and current terminal region 1605. The voltage applied to current terminal region 1607 is sufficiently positive so that it effectively masks or shadows any charge present in charge storage location 1711. In

this way, the current through the channel region is primarily affected by the charge stored in location 1709 and not by the charge stored in any other charge storage location.

To erase a charge stored in a charge storage location, a hot hole injection technique may be utilized. For example, to erase the charge stored in charge storage location 1709, a negative voltage ($-V_{pp}$) is applied to gate structure 1503 and a positive voltage (V_{pp}) is applied to current terminal region 1605, the current terminal adjacent to charge storage location 1709. A ground potential (V_{ss}) is applied to current terminal region 1605 and gate structure 1505.

In another embodiment, the charge storage locations of structure 1621 may be erased at the same time by applying a negative voltage ($-V_{pp}$) to gate structures 1503 and 1505 and a positive voltage (V_{pp}) to current terminal regions 1605 and 1607.

In other embodiments, other program, read, and/or erase techniques may be utilized for programming, reading and/or erasing the charge in the charge storage location of transistor structure 1621. For example other conventional techniques for reading a non volatile memory cells having two storage locations may be used.

In other embodiments, transistor structure 1621 may be utilized such that it implements only two charge storage locations. In one such embodiment, the first charge storage location is located in charge storage structure 1305 and the second charge storage location is located in charge storage structure 1307. With these embodiments, transistor structure 1621 is utilized as two functional transistors with each functional transistor including a charge storage location. In one example of such an embodiment, the charge storage layer would be made of conducting material (e.g. polysilicon) e.g. as with a floating gate transistor.

In other embodiments having only two charge storage locations, each charge storage structure (1305 and 1307) would independently be able to store a charge, but transistor structure 1621 would be read as a single functional transistor having 4 voltage threshold levels. The voltage threshold would be a function of the charge stored in both the charge storage structures. In this embodiment, the charge storage structures would be programmed with different voltages applied to the gates structures. The transistor structure would be read with a single voltage

applied to both gate structures. In some of these embodiments, the gate structures would be preferably of different conductivity types or would have different work functions.

In other embodiments, a transistor structure having gate structures adjacent to the sidewalls of the channel region may have other configurations. For example, the width, length, and/or height of the channel region 1725 may be of other dimensions. Also in other embodiments, multiple transistor structures may be linked together wherein each transistor structure shares a current terminal region (e.g. 1607) with the adjacent transistor structure. The channel regions (e.g. 1725) and the gate structures (e.g. 1503 and 1505) would be located between the shared current terminal regions (e.g. 1607 and 1605). An example of such an implementation may be represented by the array shown in FIG. 18 wherein the current terminal region of one transistor structure is serves as the current terminal of another transistor structure. For example, referring to FIG. 16, a second intermediate structure (not shown) would extend from end structure 1630 in the opposite direction (to the left relative to the view shown in FIG. 17) as intermediate structure 1631 of structure 1104 extends from end structure 1630. A third intermediate structure (not shown) would extend from end structure 1629 in the opposite direction (to the right relative to the view shown in FIG. 17) as intermediate structure 1631 extends from end structure 1629. A pair of gate structures similar to gate structures 1503 and 1505 would be adjacent to each sidewall of the second intermediate structure and third intermediate structure, similar to the position of gate structures 1503 and 1505 with respect to intermediate structure 1631.

In other embodiments, the gate structures 1503 and 1505 may have different conductivity types. This may be accomplished in one embodiment by angled implantation of different dopant species. For example gate structure 1505 may be implanted with a P+ dopant and gate structure 1503 may be implanted with an N+ dopant.

FIG. 18 is a circuit diagram of a non volatile memory array implementing the transistor structure 1621 as a memory cell including four storage locations (1713, 1709, 1715, and 1711). In one embodiment, array 1801 is a non volatile memory array of an integrated circuit device. Array 1801 includes a number of memory cells with each cell (e.g. 1809, 1805, 1807)

implementing a transistor structure similar to transistor structure 1621. Each cell includes four storage locations similar to storage locations 1713, 1709, 1715, and 1711.

The gate structures (e.g. 1505 and 1503) of each cell are coupled to a word line. For example, gate structure 1505 is couple to word line WL0 and gate structure 1503 is coupled to word line WL1. Each current terminal region of a memory cell is coupled to a bitline. For example, terminal contact 1611 of terminal region is coupled to bitline BL1 and current terminal contact 1613 is coupled to bitline BL2. The bitlines (BL0, BL1, BL2, and BL3) and the word lines (WL0, WL1, WL2, and WL3) of array 1801 are couple to conventional memory array control circuitry (not shown) for controlling the voltages of the lines. The memory cells are arranged in array 1801 in rows and columns. In the embodiment shown, cells 1809 and the cell of transistor structure 1621 are in the same row, and cells, 1809 and 1807 are in the same column.

FIG. 19 sets forth the voltages applied to the bitlines and word lines shown in FIG. 18 for programming, erasing, and reading storage location 1713. In one embodiment, $V_{pp} = 8.0V$, $V_{ss} = 0$, and $V_{dd} = 4.0$. To read storage location 1713, BL1 is coupled to a sense amplifier (not shown), as designated by "SA" in the table of FIG. 19, to determine whether the transistor has been turned on or not. Whether a transistor has been turned on or not is dependent upon whether a charge is stored at the charge storage location (e.g. 1713) being read. To program location 1713, a voltage of $V_{PP}/2$ is applied to bitline BL1 and all bitlines located before BL1 (e.g. BL0) so that locations having a gate coupled to word line WL0 located before bitline BL1 (e.g. charge storage location 1821) are not programmed. A ground voltage V_{SS} is applied to all bitlines located after BL1 (e.g. BL2 and BL3) so that no charge storage locations located after bitline BL2 (e.g. 1823) are inadvertently programmed.

In other embodiments, the charge storage locations of array 1801 may be erased in a block erase function. In these embodiments, a positive voltage is applied to all bitlines and a negative voltage is applied to all word lines.

FIG. 20 sets forth voltages applied to the bitlines and word lines shown in FIG. 18 for programming, erasing, and reading storage location 1711.

As shown in the tables of FIGs. 19 and 20, the gate of a cell opposite of the charge storage location being programmed, erased, or read is biased at ground (VSS) during these operations. For example, gate structure 1503, which is opposite of charge storage location 1713, is biased at VSS during program, erase, and read operations of location 1713.

5 FIGs. 21 and 22 set forth voltages that are applied to the bitlines and word lines of array 1801 in another embodiment for programming, erasing, and reading the charge storage locations of 1801. In this embodiment, the opposing gate to the charge storage location of a cell being programmed is biased at the opposite voltage of the gate of the cell associated with that location. For example, referring to FIG. 21, to program location 1713, a positive voltage VPP is applied to
10 the word line (WL0), which is coupled to gate structure 1505 and is associated with charge storage location 1713, and -VPP is applied to word line WL1, which is coupled gate structure 1503 and is opposite to charge storage location 1713. In this embodiment, the width and conductivity of the channel regions of the transistor structures are such that the potential of the channel region adjacent to a gate structure is influenced by the opposing gate structure.

15 Because a negative program voltage can be applied to the opposing gate of a charge storage location being programmed, the voltage applied to the gate associated with the cell being programmed may be reduced accordingly. For example, in one embodiment, VPP may be 6.0 volts. Accordingly, because this embodiment allows for a reduction in the program voltage, lower programming voltages may be utilized. In some embodiments, reducing the programming
20 voltage may allow for a reduction in the area required for circuitry to provide the programming voltage.

 Another advantage that may occur from using a transistor with gate structures adjacent to opposing sidewalls in a memory array is that the opposite gate of a charge storage location can provide a transistor such as e.g. a FinFET with a voltage control circuit that effectively acts like
25 as a well voltage control circuit for a planar CMOS transistor. However, unlike the well voltage control circuit for planar CMOS transistors, the voltage of the opposing gate can be controlled independently of gates in other rows of the array. This may allow for the use of more advanced program and erase techniques for an array than would be possible with other types of charge storage transistors.

One advantage that may occur with the array shown in FIG. 18 is that more charge storage locations may be implemented in a given area than with planar CMOS NVM cells. Furthermore, with the array of FIG. 18, because 4 independent storage locations are programmable utilizing just two current terminal contacts, the transistors may be more closely placed in an array. In some embodiments, a transistor structure similar to transistor structure 1621 may be easily implemented in an integrated circuit having devices implementing FinFET technology or other types of silicon on insulator technology.

In another embodiment, transistor structure 1261 may be modified to have only one charge storage structure between a gate and the sidewall of the channel region. With one embodiment of such a transistor, the opposing sidewall would not have a charge storage structure between it and the opposing gate. The opposing gate would serve as an effective well bias voltage control circuit.

Furthermore, transistor structures such as those describe above may be implemented in memory arrays having other configurations. Also in other embodiments, a memory cell having two independent gate structures adjacent to opposing sidewalls of a semiconductor structure and having charge storage locations located between the gate structures and the sidewalls maybe made by other semiconductor processes other than that set forth in this specification, including other conventional processes for forming independent gate structures.

FIG. 23 illustrates a schematic diagram of a mixer circuit 2000 in accordance with the present invention. Mixer circuit 2000 includes identical mixer portions 2001 and 2003. Mixer portion 2001 includes resistance element 2002 and transistor 2006. Transistor 2006 includes gate terminals 2010 and 2012. Mixer portion 2003 includes resistance element 2004 and transistor 2008. Transistors 2006 and 2008 are multiple independent gate finFETs as described above and having a cross section as illustrated in FIG. 9. Transistor 2008 includes gate terminals 2014 and 2016. In mixer portion 2001, resistance element 2002 has a first terminal coupled to a power supply voltage terminal labeled "VDD" and a second terminal for providing an output signal labeled "VO(t)". Transistor 2006 has a first gate 2001 for receiving a first time varying signal labeled "V1(t)", a second gate 2012 for receiving a second time varying signal labeled "V2(t)", a first source/drain terminal coupled to the second terminal of resistance element 2002,

and a second source/drain terminal coupled to a power supply voltage terminal labeled “VSS”. Mixer portion 2003 is identical to mixer portion 2001 except that signals VO(t)*, V1(t)*, and V2(t)* are logical complements of the same signals having the same name but lacking the asterisk (*). That is, signal VO(t) is 180 degrees out of phase with signal VO(t)*, signal V1(T) is 180 degrees out of phase with signal V1(t)*, and signal V2(t) is 180 degrees out of phase with signal V2(t)*. In the illustrated embodiment, VDD is a positive power supply voltage of about 1 to 1.5 volts and VSS is coupled to ground. Transistors 2006 and 2008 both have fully depleted channels and symmetrical gate and source/drain regions. Resistance elements 2002 and 2004 function as loads for transistors 2006 and 2008, respectively, and can be either active or passive loads. For example, resistance elements 2002 and 2004 may be polysilicon resistors (passive) or transistors (active). Also, in another embodiment, resistance elements 2002 and 2004 may be implemented using a multiple independent gate finFET as illustrated in FIG. 9.

In operation, input signals V1(t) and V2(t) are provided to gates 2010 and 2012, respectively, and input signals V1(t)* and V2(t)* are provided to gates 2016, respectively. Input signal V1(t) may be, for example, an oscillator signal and input signal V2(t) may be, for example, an analog signal or a digital signal from an antenna or a baseband circuit. In the illustrated embodiment, mixer circuit 2000 is a square law mixer circuit where the transistors operate in saturation mode. Output signal VO(t) = kV1(t)V2(t). Constant k depends on the gain of the mixer. The channel region between the two gates is modulated by the input signals provided to the gates. A drain current I_D through resistance element 2002 is

$$I_D = \mu C_{ox} / 2 (W/L) (V_{GS1} + V_{GS2} - V_T)^2$$

where μ is a mobility constant, C_{ox} is a gate oxide capacitance, W is the gate width, L is the gate length, V_{GS1} is the gate source voltage of one of the two gates, V_{GS2} is the other gate voltage, and V_T is the threshold voltage. Note that in another embodiment, mixer 2000 may be a phase detector used to detect a difference in phase between two time varying input signals.

Mixer circuit 2000 provides the advantages of having fully symmetrical independent input gates. The transistor does not suffer from unpredictable body effects such as floating body and source-drain coupling of back bias. The gate lengths of the transistors may be changed

without a process change, providing a highly linear mixer. Also, because a transistor stack is not used as in some prior art mixers, mixer circuit 2000 can operate at low power supply voltages.

To achieve desired drive current in, for example, a mixer application, multiple parallel connected transistors may be used.

5 FIG. 24 illustrates a top down layout view of a transistor structure 2100 used in mixer circuit 2000 of FIG. 23. Transistor structure 2100 includes three multiple independent gate FETs connected in parallel. Each transistor of the plurality of transistors is the same as the transistor described in the discussion of FIG. 9. Transistor 2100 includes a first gate structure 2102 and a second gate structure 2104. First gate structure 2102 includes gates 2108, 2110, and 2112
10 electrically connected together, where each of the gates is adjacent to the sidewalls of the fin structure 2106 and between source and drain contacts. Second gate structure includes gates 2114, 2116, and 2118. Fin structure 2106 includes source/drain terminals 2120, 2122, 2124, and 2126. Each source/drain terminal is accessed via a corresponding one of contacts 2136, 2138, 2140, and 2142. Channel regions are formed between the source/drain terminals and are
15 controlled by the gates. For example, in FIG. 24, a channel region exists between source/drain terminals 2120 and 2122 controlled by gates 2114 and 2108. In FIG. 24 there are three parallel connected multiple independent gate transistors. However, in other embodiments, there may be only one, or more than three, parallel connected transistors depending on the desired W/L (width/length) ratio. Likewise, gate structure 2102 is accessed via contacts 2130, 2132, and
20 2134, and gate structure 2104 is accessed via contacts 2144, 2146, and 2148. The contacts couple to metal layers implemented above the gate and the source/drain terminal. Note that in the illustrated embodiment, three contacts are shown for each gate structure, however, there may be any number of contacts as long as an acceptable electrical connection can be made.

 The source/drain regions are made symmetrical in the illustrated embodiment, thus
25 allowing the gate length L to be changed without a corresponding process change. In the illustrated embodiment, the gate length L is the same for all of the parallel connected transistors, however, in other embodiments, the gate length L may be different for the different portions. One advantage of the transistor of FIG. 9 is that the gate length L may be easily changed with just a layout change. That is, no process change is necessary to change the gate length. Also,

because the gates are symmetrical, the source/drain terminals are interchangeable. In addition, the channel regions between source/drain terminals of fin structure 2106 may have different widths in other embodiments. In the illustrated embodiment, the distance between the source/drain terminals are the same, however, in other embodiments, the distance between the source/drain terminals may be different.

While particular embodiments of the present invention have been shown and described, it will be recognized to those skilled in the art that, based upon the teachings herein, further changes and modifications may be made without departing from this invention and its broader aspects, and thus, the appended claims are to encompass within their scope all such changes and modifications as are within the true scope of this invention.